

Remarks

Reconsideration of this application as amended for prosecution is respectfully requested.

The Examiner objected to the drawings. The brief description of the drawings has been amended. Please replace page 5 of the application with the amended brief description of the drawings.

The Examiner requested that Applicants add a "Summary of the Invention" description to the application. However, Applicants would like to kindly point out that both the M.P.E.P. and 37 C.F.R. §1.73 do not require the presence of a "Summary of the Invention" in a patent application. They merely indicate where in the application the "Summary of the Invention" should be placed if Applicants were to elect to include one.

In particular, 37 C.F.R. §1.73 only states that "[a] brief summary of the invention ... should precede the detail description." 37 CFR § 1.73 does not state "must" or "shall." Accordingly, Applicants have elected not to include a "Summary of the Invention" as this is within the discretion of Applicants.

The Examiner rejected Claims 1-14, 19-21, and 25-29. Claims 1-7, 9-14 and 25-29 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 6,088,264 of Hazen ("Hazen") in view of U.S. Patent 6,201,739 of Brown ("Brown"). Claims 8 is rejected under 35 U.S.C. § 102(e) as being anticipated by Hazen. Claims 19-21 are rejected under 35 U.S.C. § 102(e) as being anticipated by Brown.

Applicants submit that Claim 1 is patentably distinguished over Hazen in

view of Brown. Claim 1 includes the limitations:

dividing the memory device into k partitions,
wherein k is an integer greater than or equal to two;
performing code operations from m code partitions
out of k total partitions, wherein m is an integer
greater than or equal to one;
performing data operations from n data partitions
out of k total partitions through low level functions
accessed from the code partitions at approximately
the same time as the code operations are performed
from the m code partitions, wherein n is an integer
greater than or equal to one; and
suspending the data operations of the n data
partitions if a preempting operation is detected.

(Claim 1) (emphasis added).

Hazen discloses a flash memory partitioning for read-while-write operation that permits simultaneous access to more than one subsection of the flash memory. (Hazen, column 2, lines 23-38). Hazen further discloses an example of a three partitioned flash memory device that has code executed from a first partition, while updating data in a second partition. (Hazen, column 3, lines 55-59). Hazen, however, does not disclose suspending the data operations of the n data partitions if a preempting operation is detected.

Brown discloses using a pin to preempt an operation in a nonvolatile writeable memory.

It is respectfully submitted that Hazen does not teach or suggest a combination with Brown and that Brown does not teach or suggest a combination with Hazen. It would be impermissible hindsight based on applicants' own disclosure to incorporate the partitioned flash memory of Hazen into the preemption pin of Brown.

Moreover, such a combination would still lack the limitation of **suspending the data operations of the n data partitions if a preempting operation is detected**. The assertion of the suspend pin 480 of Brown does not depend on whether a preempting operation is detected. In addition, the suspend pin 480 of Brown is coupled to provide an input to the suspend/resume circuitry 482. Brown does not suggest suspending the data operations of n data partitions out of k total partitions as set forth in Claim 1.

Further, Hazen and Brown do not disclose performing data operations from n data partitions out of k total partitions through **low level functions accessed from the code partitions**.

Given that Claims 2-7 depend from Claim 1, applicants submit that Claims 2-7 are patentably distinguished over the references cited by the Examiner.

Applicants submit that Claim, 8 as amended, is not anticipated under 35 U.S.C. § 102(e) by Hazen. Claim 8 includes the limitations:

means for partitioning a memory device into a first plurality of partitions for storing code and a second plurality of partitions for storing data to enable multiple operations to be performed on a memory device at the same time;

means for setting each of the partitions to a status mode to track operations performed on the memory device; and

means for determining if a first requested operation has priority over a second requested operation.

(Amended Claim 8) (emphasis added).

In contrast, Hazen discloses a three partitioned flash memory device. A

first partition, partition A 310, may be used to store data. A second partition, partition B 315, may be used to store code. A third partition, partition C, may be used to permit updating of the code. (Hazen, column 3, lines 44-49). Hazen further discloses a status register 335 associated with partition A, a status register 340 for partition B, and a status register 345 for partition C. (Hazen, column 4, lines 7-14).

Hazen, however, does not disclose a means for determining if a first requested operation has priority over a second requested operation as set forth in Claim 8.

Moreover, even if Hazen did disclose a means for determining if a first requested operation has priority over a second requested operation, Hazen fails to disclose setting each of the partitions to a status mode. The partitions of Hazen are not set to a status mode prior to an indication of the status by status registers 335, 340, and 345.

Given that Claims 9-10 depend from Claim 8, applicants submit that Claims 9-10 are patentably distinguishable over the references cited by the Examiner.

Applicants submit that Claim 11 is patentably distinguishable over Hazen and Brown. Claim 11 includes the limitations:

- a data partition;
- a code partition;
- a status mode to provide a partition status from the memory array if a task request is received by the data partition, wherein if the partition status is busy, an algorithm in the code partition determines whether the task request preempts an existing task;
- a read mode to enable code and data to be read

from the memory array; and
a write mode to enable data to be written to the
memory array.

(Claim 11) (emphasis added).

Hazen discloses a multi-partitioned flash memory device... Each partition has associated an X decoder and a Y selector... Having multiple X selectors and Y decoders permits simultaneous access to more than one subsection of the flash memory. For example, while partition A may be erased, partition B may simultaneously be read... A memory in partition A may be written to, while a memory block in partition B is erased. (Hazen, column 2, lines 25-42). Thus, Hazen only discloses the write operation and read operation itself.

Brown discloses a program suspend latch 376e that latches a signal 372e to suspend a program operation. This occurs when a suspend command is written to the command decoder 370 while a program operation is being performed or when a unique program suspend command, different from an erase suspend command, is written to the command decoder. (Brown, column 6, line 47 to column 7, line 18).

It is respectfully submitted that Hazen does not teach or suggest a combination with Brown and that Brown does not teach or suggest a combination with Hazen. It would be impermissible hindsight based on applicants' own disclosure to incorporate the partitioned flash memory of Hazen into the suspend operation of Brown.

Moreover, such a combination would still lack the limitation of a memory array having a read mode to **enable** a read operation and a write mode to

enable a write operation.

Further, even if Hazen or Brown did disclose a read mode to enable code and data to be read from the memory device and a write mode to enable data to be written to the memory device, Hazen and Brown do not disclose a status mode to provide a partition status from the memory array if a task request is received by the data partition, wherein if the data partition is busy, an algorithm in the code partition determines whether the task request preempts an existing task.

The Examiner alleges, "It is inherent that an algorithm exists for a task being preempted as this is a normal program activity for when a conflict for using the same memory location is executed..." (2/26/04 Office Action, page 10, lines 5-7). Even if the Examiner's assertion is true, Brown does not disclose the possibility of one operation having preempting status over another operation. The command latches 376a-n of Brown are automatically latched upon assertion of the write enable pin 330. The program suspend latch 376e latches a signal 372e to suspend a program operation. Thus, applicants respectfully disagree that it is inherent that an algorithm in the code partition determines whether the task request preempts an existing task.

Given that Claims 12-14 depend from Claim 11, applicants submit that Claims 12-14 are patentably distinguishable over the references cited by the Examiner.

Applicants submit that Claim 19 is not anticipated under 35 U.S.C. § 102(e) by Brown. Claim 19 includes the limitations:

a memory device having a code partition and a data partition, wherein the code partition comprises a low level function that is performed on data stored in the data partition; and

a flag to indicate when a suspend operation has occurred.

(Claim 19) (emphasis added).

In contrast, Brown discloses a flash EPROM that stores both code and data. (Brown, column 9, line 49). The Examiner alleges that column 5, lines 46-67 of Brown discloses “a memory device having a code partition and a data partition...” (2/26/04 Office Action, page 6, lines 12-13). However, this citation of Brown merely discloses a memory array control circuitry 140 that includes erase circuitry 190 and program circuitry 194 to perform operations on memory array 150. The memory array 150 of Brown does not have a code partition and a data partition, wherein the code partition comprises a low level function that is performed on data stored in the data partition.

Given that Claims 20-21 depend from Claim 19, applicants submit that Claims 20-21 are not anticipated under § 102(e) by the reference cited by the Examiner.

Applicants submit that Claim 25 is patentably distinguished over Hazen and Brown. Claim 25 includes the limitations:

running a first operation of a first partition of a memory array;

running a first operation of a second partition of the memory array;

requesting a second operation to be performed on the second partition; and

determining from the first operation of the first partition if the second operation of the second partition has a higher priority than the first operation of the second partition.

(Claim 25) (emphasis added).

Hazen discloses a three partitioned flash memory device having a first partition to store data, a second partition to store code, and a third partition to permit updating of the code. (Hazen, column 3, lines 44-49).

Brown discloses an erase circuitry 190 that includes erase suspend circuitry 192 and program circuitry 194 that includes program suspend circuitry 195. (Brown, column 5, lines 54-59).

It is respectfully submitted that Hazen does not teach or suggest a combination with Brown and that Brown does not teach or suggest a combination with Hazen. It would be impermissible hindsight based on applicants' own disclosure to incorporate the three partitioned flash memory device of Hazen into the suspend circuitry of Brown.

Moreover, such a combination would still lack the limitation of determining from the first operation of the first partition if the second operation of the second partition has a higher priority than the first operation of the second partition. The Examiner alleges that "being able to suspend operations depends upon which operations being executed which inherently requires determining the priority of execution of the code." (2/26/04 Office Action, page 11, lines 10-12). However, Brown does not disclose a first memory partition or a second memory partition. Brown also does not disclose a first operation of the first partition, or a first operation and a second operation of a second partition. Even if Brown disclosed these limitations, applicants respectfully disagree that suspending an operation inherently requires determining priority. It is possible to perform a suspend

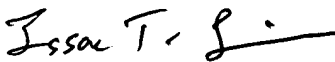
operation without first determining whether the second operation of the second partition has a higher priority than the first operation of the second partition.

Given that Claims 26-29 depend from Claim 25, applicants submit that Claims 26-29 are patentably distinguished over the references cited by the Examiner.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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Issac T. Lin
Reg. No. 50,672

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300